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10/699,909	11/03/2003	Jason Harold Culler	200310794-1	5350

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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	PAPER NUMBER
2116	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/699,909	CULLER, JASON HAROLD	
	Examiner	Art Unit	
	FAHMIDA RAHMAN	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-15,18,20-28,30-35,37 and 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-15,20-28,30-35,37 and 38* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to communications filed on 4/15/08.

2. Claim 30 has been amended, no new claims have been added and claims 12, 16-17, 19, 29, 36 have been cancelled. Thus, claims 1-11, 13-15, 18, 20-28, 30-35, 37-38 are pending.

3. Applicant's arguments are moot in view of new grounds of rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 9, 11, 13, 14, 25, 26-28, 30-35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Majos (US Patent 6701445), in view of Dieguez (US Patent 7127022).

For claim 1, Majos teach the following limitations:

A system comprising:

a sample network (1) **that provides plural samples** (Q1, Q2, Q3, Q4) **of an input signal state** (1H) **for different time instances of the input signal** (H is sampled for each transition of the incoming data signal Din; lines 15-17 of column 5; Q1 and Q3 are apart by dt), **each of the plural samples corresponding to the input signal delayed**

by a known amount of time (Q1 is delayed by "0" corresponding to input signal H when Din transitions and Q3 is delayed by dt corresponding to input H when Din transitions)**; and a detector** (3) **that determines the frequency for the input signal** (H+, H-) **based on samples of the input signal state received by the detector for different time instances of the input signal residing within one period of the input signal** (dt can be atmost half period of H. Thus, Q1 and Q3 resides within one period of H)**, and the known amount of time for each of the plural samples** ("0" delay and "dt" delay is known)**, the detector provides a value that represents the frequency of the input signal** (H+, H- represents frequency of H with respect to Din. For example, when H+, H- is 00, H and Din are substantially at the same frequency); **a module** (4) **that provides a signal** (4 to 5) **based on a comparison of the value of the frequency for the input signal and a value of a desired frequency** (4 to 5 is based on comparison between Din and H as shown in Table. Frequency of Din is the desired frequency); **and a controller** (5 and 6) **operative to implement adjustments to a clock signal based on the signal** (H is adjusted according to lines 50-51 of column 4).

However, detector 3 provides a value that represents an indication of frequency, or a frequency value, not the determined frequency as recited in claim 1. Table shown in column 7 mentions that H+H- = 00 means H and Din are at substantially same frequency (lines 15-20 of column 7). In addition, 4 is labeled as updown counter, not a comparator.

Majos provides second embodiment where Din is a known frequency (Fig 5 shows Hr as Din. Lines 10-42 of column 11 mention that how Hr can be programmed). Thus, when H is equal to Hr, the frequency of H is determined and known, which is provided by the detector as H+H- = 00).

Dieguez teaches a comparator (204) that provides a comparator signal (signal from 204 to 207) based on a comparison (lines 24-40 of column 10 mention that 204 compares the number of phase lead error to phase lag error).

Majos does not explicitly mention that the frequency value represents a frequency value of the signal. Dieguez teaches that the up/down signal from the phase and frequency detector includes the information about difference between two clock signals (lines 40-45 of column 6).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Majos and Dieguez. One ordinary skill would be motivated to have the determined frequency value as that provide more information. As the second embodiment of Majos (Fig 5) shows that the reference frequency Hr is known and programmable (lines 59-63 of column 8), the combined teachings of Dieguez provides the determined frequency value of the signal. The up/down signal from Dieguez includes the difference between two frequency. When Hr is known, the signal provides determined frequency of the other signal.

For claims 2, 9, 11, 14-17 in Majos are the storage elements.

For claim 13, oscillator VCO in Majos generates clock signal H.

For claim 14, Majos does not explicitly mention about IC chip. Examiner takes an official notice that the system implemented within the IC chip is well known in the art. An ordinary skill in the art would have been motivated to implement the system within the IC chip for many reasons, such as, to make commercially available to the customers.

For claim 25, Majos teaches the following limitations:

A frequency detection system comprising:

means for sampling (1) **an input signal** (H) **having an unknown frequency and for providing plural indications of signal state** (Q1, Q2, Q3, Q4) **associated with different time instances of the input signal** (H is sampled for each transition of the incoming data signal Din; lines 15-17 of column 5; Q1 and Q3 are apart by dt) **delayed for different amounts of time** (Q1 is delayed by "0" corresponding to input signal H when Din transitions and Q3 is delayed by dt corresponding to input H when Din transitions)**; and means for determining a frequency** (3) **for the input signal based on I) the plural indications of signal state received by the means for determining, that correspond to time instances of the input signal residing within a single period of the input signal** (dt can be at most half period of H. Thus, Q1 and Q3

resides within one period of H) **and ii) the known amounts of time** ("0" delay and "dt" delay is known)**; means for comparing** (3 and 4) **the frequency value relative to a desired frequency value** (signal 4 to 5 is based on comparison between Din and H as shown in Table. Frequency of Din is the desired frequency)**; and means for controlling the frequency of the input signal based on the comparison of the frequency of the input signal and the desired frequency** (H is adjusted according to lines 50-51 of column 4)**.**

However, detector 3 provides a value that represents an indication of frequency, or a frequency value, not the determined frequency as recited in claim 25. Table shown in column 7 mentions that H+H- = 00 means H and Din are at substantially same frequency (lines 15-20 of column 7).

Majos provides second embodiment where Din is a known frequency (Fig 5 shows Hr as Din. Lines 10-42 of column 11 mention that how Hr can be programmed). Thus, when H is equal to Hr, the frequency of H is determined and known, which is provided by the detector as H+H- = 00).

Majos does not explicitly mention that the frequency value represents a frequency value of the signal. Dieguez teaches that the up/down signal from the phase and frequency detector includes the information about difference between two clock signals (lines 40-

45 of column 6). Therefore, the up/down signal is the means for providing a corresponding frequency value for the determined frequency.

Although Majos provides the means for comparing (table in column 7), means for determining and comparing in Majos share the same circuitry (3). Dieguez teaches a comparator (204) that provides a comparator signal (signal from 204 to 207) based on a comparison (lines 24-40 of column 10 mention that 204 compares the number of phase lead error to phase lag error).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Majos and Dieguez. One ordinary skill would be motivated to have the determined frequency value as that provide more information. As the second embodiment of Majos (Fig 5) shows that the reference frequency Hr is known and programmable (lines 59-63 of column 8), the combined teachings of Dieguez provides the determined frequency value of the signal. The up/down signal includes the difference between two frequency. When Hr is known, the signal provides determined frequency of the other signal.

For claim 26, delaying means are selected parts of sampling means.

For claims 27 and 28, Fig 2 shows the storage elements and delaying the clock signal to provide the activation signal.

For claim 30, Majos teaches a method comprising:

- **sampling** (1 in Fig 1) **a signal** (H in Fig 1) **at predetermined and spaced apart time intervals** (H is sampled for each transition of the incoming data signal Din; lines 15-17 of column 5; Q1 and Q3 are apart by dt) **to provide a plurality of output samples indicative of signal state for different time instances of the signal** (Q1, Q2, Q3, Q4 are plural samples)**;**
- **determining a frequency value** (H+, H-) **for the signal based on (i) the output samples received at a detector** (3) **that correspond to time instances of the signal residing within a single period of the signal** (dt can be atmost half period of H. Thus, Q1 and Q3 resides within one period of H)**, and (ii) the predetermined and spaced apart time intervals** (Q1 is sampled when Din transitions and Q3 is sampled after dt interval. 3 detects frequency value H+ and H- based on Q1, Q3)**;**
- **controlling an oscillator** (VCO in Fig 1) **to provide the signal at a frequency based on a comparison of the frequency value for the signal relative to a desired frequency value** (4 performs a comparison between desired HE and H+/H-)

Majos does not explicitly mention that the frequency value represents a frequency value of the signal. Dieguez teaches that the up/down signal from the phase and frequency detector includes the information about difference between two clock signals (lines 40-45 of column 6).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Majos and Dieguez. One ordinary skill would be motivated to have the determined frequency value as that provide more information. As the second embodiment of Majos (Fig 5) shows that the reference frequency Hr is known and programmable (lines 59-63 of column 8), the combined teachings of Dieguez provides the determined frequency value of the signal. The up/down signal includes the difference between two frequency. When Hr is known, the signal provides determined frequency of the other signal.

For claims 31, 32 and 35, 14-17 in Majos are the storage elements and clock edges are provided to storage elements.

For claim 33, 12 in Majos delays the clock to provide the clock edges.

For claim 34, dt in Majos is known. H is delayed by dt in 16 to establish time intervals such as transition in Din and dt+ transition in Din.

For claim 37, oscillator in Majos does not change when H+, H- is 00.

5. Claims 3-8, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Majos (US Patent 6701445), in view of Dieguez (US Patent 7127022), in view of Lee et al (US Patent 6326826).

For claim 3, Majos does not teach plurality of delay elements providing respective delayed clock signals to clock the storage elements. Lee et al teach plural storage elements (22') to provide samples (EDGE[N]) corresponding to plural samples of REF_CK at the output of delay elements. The system of Lee et al further comprises delay elements (Delay0-Delay6) for delayed clock signal (CK[N]) to clock storage 22' to sample input signal at different time interval (the plural samples of input signal just at the end of delay elements are sampled at different time interval) and thereby providing plural samples of the input signal state to the decision logic 23.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Majos and Lee et al. One ordinary skill would be motivated to use storage elements with delay elements when sequential design is desirable.

For claim 4, input signal REF_CK of Lee is delayed by delay elements.

For claims 5 and 6, clock signal activates the storage elements in Fig 2 of Lee. However, neither Majos nor Lee teaches that the oscillator generates the clock signal that is activating the storage.

Examiner takes an official notice that the oscillator generating clock signal is well known in the art. An ordinary skill in the art would have been motivated to have an oscillator providing the clock signal REF_CK, since oscillator provides an on-chip generation of clock signal. The oscillator generated signal is divided by PLL and therefore, oscillator generated clock typically has higher frequency that the supplied clock.

For claim 7, Lee et al teach 7 storage elements (22') to provide samples (EDGE[N]) corresponding to plural samples of REF_CK at the output of 7 delay elements. The system of Lee et al further comprises delay elements (Delay0-Delay6) with fixed known amount of delay for delayed clock signal (CK[N]) to clock storage 22' to sample input signal at different time interval (the plural samples of input signal just at the end of delay elements are sampled at different time interval) and thereby providing plural samples of the input signal state to the decision logic 23.

For claim 8, delay components are in series. The oscillator can be used to generate a clock from which REF_CK can be generated.

For claim 10, H is a direct input to 14 and 16.

6. Claims 15, 20-24, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Majos (US Patent 6701445), in view of Lee et al (US Patent 6326826).

For claim 15, Majos teaches the following:

A system comprising:

a plurality of storage elements (14, 15, 16, 17 of Fig 2), **the plurality of storage elements being clocked to latch** (Fig 2) **different time instances of an input signal** (1H in Fig 2) **to provide corresponding output samples of the input signal** (Q1(Tn), Q2 (Tn-k), Q3(Tn+dt), Q4(Tn-k+dt) of Fig 2) **sufficient for determining a frequency value** (H+, H-) **of the input signal** (3 determines frequency value H+, H- from Q1-Q4); **a delay element** (output of 10 goes to delay 12) **associated with at least a substantial number of the storage elements** (11-12 are associated with 14-17), **the delay element delaying a sample signal** (output of 10) **by a respective known amount of time** (delayed by "dt") **to provide a respective clock signal** (Fig 2) **that clocks a respective one of the at least a substantial number of the storage elements** (clock signals clock 14-17 in Fig 2) **to latch a respective one of the different time instances of the input signal** (the different instances of input signal is latched as shown in Fig 2) **to provide at least a portion of the corresponding output samples** (Fig 2); **and a detector** (3) **that provides a frequency value** (H+, H-) **for the input signal** (combination of H+, H- is a frequency value for the input signal as the combination provides indication of frequency of H as explained in table of column 7) **based (i) on output samples that correspond to different time instances of the**

input signal (Q1-Q4 are input to 3 as shown in Fig 1) **and (ii) the known amount of time for each respective delay element** (samples are dependent on the "0" delay and "dt" delay and 3 provides frequency value based on samples, the detector provides frequency value based on output samples and the known amount of time).

Majos does not mention about delay path from 10 to 14. However, that can be thought as a delay element with "0" delay. Although the "0" delay path 10 to 14 can be thought as a delay element, Examiner cites Lee to provide a better explanation. Lee teaches delay elements delaying sample signal. Therefore, one ordinary skill may put one more delay element in the path of 10 to 14 for a different design to meet all the limitations of claim 15. Such a modification is possible within the scope of Majos and can provide better sampling of H.

For claim 20, lines 60-62 of Majos mention that sample signal is a clock signal. However, it does not mention oscillator.

Examiner takes an official notice that the oscillator generating clock signal is well known in the art. An ordinary skill in the art would have been motivated to have an oscillator providing the clock signal, since oscillator provides an on-chip generation of clock signal.

For claim 21, Lee et al teach that the delay elements (18') provide respective clock edges (CK[1:7] in Fig 2) for activating the storage elements (22'), each of the clock edges corresponding to a different delayed version of the clock signal (11).

For claim 22, the delay elements in 11 of Lee et al are connected in series.

For claim 23, Majos teaches that the input H is directly connected to the plurality of storage.

For claim 24, 14-15 of Majos are clocked at an interval "0" and 16-17 are clocked at interval "dt" to latch the output samples to the detector concurrently.

For claim 38, H+ and H- are not expressed in unit of inverse of period. The second embodiment mentions that Fr can be expressed as unit of Hz. As H+H- = 00 implies Fr and H is at equal frequency, it is possible for one ordinary skill to express the frequency value in unit of Hz.

Response to Arguments

Applicant's arguments with respect to claims 1-11, 13-15, 20-28, 30-35, 37-38 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claim 18 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Rehana Perveen/

Supervisory Patent Examiner, Art Unit 2116

Fahmida Rahman
Examiner
Art Unit 2116